COMPLETE LISTING OF THE CLAIMS

The following lists all of the claims that are or were in the above-identified patent application. The status identifiers respectively provided in parentheses following the claim numbers indicate the current statuses of the claims.

1. (Original) An optical receiver, comprising:

a photodetector receiving an optical signal and generating a corresponding current signal;

a gain stage coupled to the photodetector receiving the corresponding current signal and converting it to a corresponding voltage signal; and

a clock data recovery (CDR) circuit directly coupled to the gain stage receiving the corresponding voltage signal, extracting clock information from the corresponding voltage signal, and regenerating the corresponding voltage signal to reduce jitter.

2. (Original) An optical receiver as in claim 1, wherein the gain stage is a transimpedance amplifier circuit having a first frequency response.

3. (Original) An optical receiver as in claim 2, wherein the transimpedance amplifier circuit and the CDR are formed on a single chip.

4. (Original) An optical receiver as in claim 2, further comprising:

a compensation circuit interposing the transimpedance amplifier circuit and the CDR circuit, the compensation circuit having a second frequency response that is approximately the inverse of the first frequency response of the tranimpedance amplifier circuit.

5. (Original) An optical receiver as in claim 2, further comprising:

a compensation circuit interposing the transimpedance amplifier circuit and the CDR circuit, wherein the compensation circuit is an equalizer.

6. (Original) An optical receiver as in claim 5, wherein the equalizer includes a synthesis filter.

7. (Original) A method for receiving an optical signal, comprising:

converting the optical signal into a corresponding current signal;

converting the corresponding current signal into a corresponding voltage signal with a gain stage;

extracting clock information from the corresponding voltage signal; and

regenerating the corresponding voltage signal to reduce jitter.

8. (Original) A method as in claim 7, further comprising:

compensating for attenuation in the corresponding voltage signal, prior to extracting clock information.

9. (Original) A method as in claim 8, wherein the gain stage is a transimpedance

amplifier having a first frequency response.

10. (Original) A method as in claim 9, wherein compensating for attenuation is performed by a compensation circuit having a second frequency response that is approximately the inverse of the first frequency response.

11. (Original) A method as in claim 7, wherein the corresponding voltage signal is equalized, prior to extracting clock information.